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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,048	04/08/2004	Sadanand V. Deshpande	FIS920030397US1	3047

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EXAMINER	
INGHAM, JOHN C	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 03/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/709,048	DESHPANDE ET AL.	
	Examiner	Art Unit	
	John C. Ingham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 12-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 12-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendments to the claims filed on 27 January 2006, canceling claims 11 and 15-25, have been entered and made of record. The 35 U.S.C. 112 rejection of claims 3 and 9 has been withdrawn.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim **2** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claim recites that second spacers are adjacent said first spacers. The claim from which it depends, claim 1, recited that an etch stop layer was between first and second spacers. The spacers cannot be adjacent if an etch stop layer is between them. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims **1-7** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kao in view of Krivokapic.

6. Regarding claim **1**, Kao discloses in Figure 5 an integrated circuit structure comprising: a substrate (100); first-type transistors (112) on said substrate, wherein said first-type transistors comprise first gate conductors (106b) and first spacers (114b) adjacent said first gate conductors; and second-type transistors (110) on said substrate, wherein said second-type transistors comprise second gate conductors (106a), said first spacers (114a) adjacent said second gate conductors.

Kao does not disclose an etch stop layer positioned on said first spacers, and second spacers on said etch stop layer.

Krivokapic teaches in Figure 2D a double spacer (items 20 and 33) on a p-channel device, separated by an oxide liner (38) that is used as an etch stop during the etch-back of spacer 33 (col 5, ln 19-23). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Krivokapic on the structure of Kao, due to the fact that an etch stop layer allows separate materials to be chosen for spacer layers in order to optimize drive current in each type of device (Krivokapic col 6 ln 1-5). The resulting structure from such a combination is a CMOS device, where the p-channel transistor contains two spacer layers to widen the channel, with an etch-stop layer between the spacers.

7. With regards to claim **2**, Kao discloses in Figure 5 the structure in claim 1, wherein said second spacers are only *adjacent* (see objection in ¶ 2 above) said first

spacers that are adjacent said second gate conductors and said second spacers are not adjacent said first spacers that are adjacent said first gate conductors.

8. Regarding claim **3**, Krivokapic discloses in Figure 2D the structure in claim 1, wherein said etch stop layer (38) is only on said first spacers (20) that are adjacent said second gate conductors (20) and said etch stop layer is not on said first spacers (33) that are adjacent said first gate conductors.

9. With regards to claim **4**, Kao discloses in Figure 5 (col 3 ln 4-8) the structure in claim 1, further comprising: first type impurity implants (108b) in areas of said substrate adjacent said first spacers (114b) of said first gate conductors; and second type impurity implants (108a) in areas of said substrate adjacent said second spacers (116b) of said second gate conductors.

10. Regarding claim **5**, Kao discloses in Figure 5 the structure of claim 4, wherein said first type impurity (108b) is spaced closer to said first gate conductors than said second type impurity (108a) is spaced from said second gate conductors.

11. With regards to claim **6**, Kao discloses in column 3, lines 4-8 the structure in claim 4, wherein said first type impurity and said second type impurity comprise source/drain impurities.

12. Regarding claim **7**, Kao discloses (col 2 ln 25-29) the structure of claim 1, wherein said first type transistors comprise NFETs and said second type transistors comprise PFETs.

13. Claims **8-10 and 12-14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kao and Krivokapic as applied to claims 1-7 above, and further in view of Ju (US 6,562,676).

14. Regarding claim **8**, Kao and Krivokapic disclose each of the elements as discussed in paragraph 5 above. Kao and Krivokapic do not disclose first-type impurity implants in areas of said substrate completely outside of said first spacers of said first gate conductors; and second type impurity implants in areas of said substrate completely outside of said second gate conductors.

Ju teaches the use of offset spacers to create source/drain extensions at optimum distances from the gate electrodes. In Figure 3, a FET is shown with source/drain regions being implanted completely outside of such an offset spacer. Figure 5 shows the same concept, applied to a FET with two spacers (see col 3 ln 45-51). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Ju on the structure disclosed by Kao and Krivokapic, in order to allow optimization of the gate to drain overlap capacitance (col 2 ln 17-18).

15. Regarding claim **9**, Kao discloses the structure as discussed in ¶ 6 above.

16. Regarding claim **10**, Krivokapic discloses the structure as discussed in ¶ 7 above.

17. Regarding claim **12**, Kao discloses that structure as discussed in ¶ 9 above.

18. Regarding claim **13**, Kao discloses the structure as discussed in ¶ 10 above.

19. Regarding claim **14**, Kao discloses the structure as discussed in ¶ 11 above.

Response to Arguments

20. Applicant's arguments with respect to claims 1-10 and 12-14 have been considered but are moot in view of the new ground(s) of rejection.

21. Applicant's arguments filed 27 January 2006 have been fully considered but they are not persuasive. Stacked structures of different materials (nitride/oxide/poly) as disclosed by Krivokapic inherently function as etch stops. Moreover, the argument that the oxide liner is used as an etch stop layer describes a functional use of the oxide layer, not a structural difference.

Conclusion

22. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John C. Ingham whose telephone number is (571) 272-8793. The examiner can normally be reached on M-F, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John C Ingham
Examiner
Art Unit 2814

jci

HOWARD WEISS
PRIMARY EXAMINER